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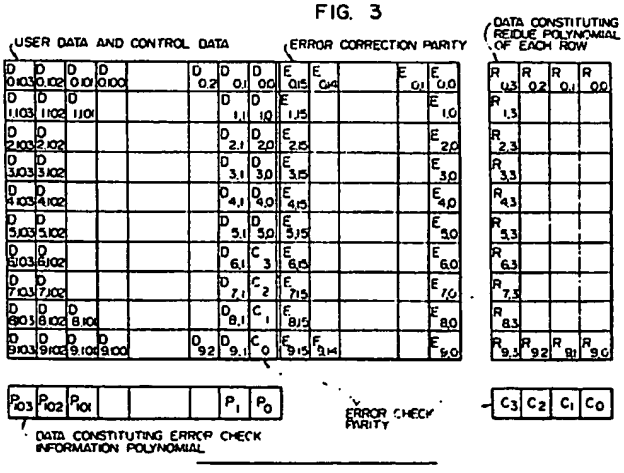
(54) A code error detecting method.

(57) In a code error detecting method, at the time of recording, a sum of n sets of information polynomials of code words of Reed-Solomon codes constituted by m data symbols ($D_{i,j}$) each of which is constituted by h binary bits and (g - m) error correction parity symbols ($E_{i,k}$) is divided by a generator polynomial to obtain a residue polynomial. The coefficients (C_3, C_2, C_1, C_0) of respective degrees of the residue polynomial thus obtained are recorded as the error check parity symbols. At the time of reproducing, data symbols ($\hat{D}_{i,j}$) constituting the n sets of information polynomials are corrected by using (g - m) error correction parity symbols ($\hat{E}_{i,k}$) A result of addition of n sets of information polynomials thus corrected is divided by a generator polynomial to obtain a residue polynomial. The coefficients ($\hat{C}_3$, $\hat{C}_2$, $\hat{C}_1$, $\hat{C}_0$)of respective degrees of the residue polynomial thus obtained are compared with the error check parity symbols ($\hat{\hat{C}}_3$, $\hat{\hat{C}}_2$, $\hat{\hat{C}}_1$, $\hat{\hat{C}}_0$), which have been subjected to correction, so as to detect the presence or absence of an error.

FIG. 3



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A CODE ERROR DETECTING METHOD

BACKGROUND OF THE INVENTION

The present invention relates to a code error detecting method of correcting data in a data file apparatus employing an optical disk of a write once type or an erasable type.

DESCRIPTION OF THE PRIOR ART

Recently, an optical disk having a characteristic capable of recording a great amount of data with a high recording density in a non-contact fashion has attracted attention in the field of memories including an auxiliary storage of a computer. As an application of the optical disk, there have been data files of a write once type in which data can be only once additionally written and of an erasable type in which data can be rewritten as many times as necessary. Efforts have been made for the development of recording methods as well as servo methods in various manufacturers and institutes.

In a data file using an optical disk, the optical disk has a diameter of 5 1/4 (5.25) or 3.5 inches and tracks in a concentric or spiral form with a track pitch of about 1.6 micrometers (μm). A track is subdivided into a plurality of sectors constituting a circumpherence thereof such that a plurality of data items including symbols each comprising eight bits are written in the sector. For example, in a case of a 5.25 inch optical disk, there are disposed 18,750 tracks, a track includes 17 sectors, and the data capacity of each sector available for the user is 1024 bytes. In a data file having such an optical disk, the rotary speed of the disk is a constant angular speed of from about 1800 rpm to about 3600 rpm, and a semiconductor laser associated with a wavelength of about 830 nanometers (nm) is adopted as a light source. With a light beam of which a light spot is focused to at most about 1 μm, data are recorded on the tracks in the form of projected or depressed portions (of the write once type) or according to directions of magnetization perpendicular to a disk surface of the optical disk (of the erasable type). In an operation to record or to reproduce data on or from the optical disks as described above, if there exists any dust, fingerprint, or damage on the disk surface, data cannot be correctly written thereon or data previously correctly written thereon cannot be appropriately read out therefrom in some cases, which is in general referred to as a code error. To cope with this code error, there are added redundant data, namely, parity data other than the data utilized by the user so as to detect a code error for error correction so that the correct data can be read even if such a code error takes place. In the data reproduction, with the error correction processing employing the above error correction code, the inherent code error data of 10^{-4} to 10^{-5} of reproduced data on an optical disk can be reduced to at most 10^{-12} after the error correction processing is effected. According to this method, there is developed the same performance as that of the hard disk conventionally used. In the data file employing an optical disk of this kind, since the minimum unit of data treated by the user is a byte, the Reed-Solomon code is used in many cases in which the error correction can be achieved in byte unit and a lot of data can be corrected with reduced redundancy. Although the Reed-Solomon code enables error detection and correction to be efficiently accomplished, it has been known that mis-detection and mis-correction of an error occur with a certain probability. Consequently, in order to increase the reliability of reproduced data with respect to the error, in addition to the error correction codes described above, there are added several bytes of error detection codes only for all data in a sector which can be used by the user, for example, 1024 bytes. The several bytes are almost ignorable as a redundancy measure. With the duplicated error detection countermeasurements, for example, even when mis-detection and mis-correction of an error occur in a error correction processing of the first stage, the code error can be appropriately detected by a code error detection processing of the second stage, thereby retaining high reliability.

As an example of the data error correction and detection method for a data file employing the optical disk, the proposal under the title of "ENCODING SPECIFICATION FOR THE X3B11-APPROVED EDAC CODE FOR 5 1/4 INCH OPTICAL STORAGE DEVICES", November 4, 1986 was submitted to the standardization committee for optical disk devices, ANSI X3B11.

According to this method, in a recording operation, a sector of user data including 1024 symbols an control data symbols are arranged in a memory area to configure a rectangular form with 10 vertical symbols X 104 horizontal symbols in which for symbols including the last data symbol in the 104-th row are assigned as the parity data for the error check of the user data. The error check parity data of this example is generated as follows. First, ten data symbols in each column among the data symbols in byte units

arranged in the first column through the 103th column are subjected to an addition of respective exclusive OR results, which means a cumulative addition of resultant data obtained by an exclusive OR operation. Further, for the 104-th column, an addition of exclusive OR results of data of six symbols excepting the error check parity is performed, thereby generating, in total, 104 error check data in byte units. An error check information polynomial is constituted by the 104 data bymols in byte unit. The error check information polynomial is divided by a generator plynomial comprising four predetermined symbols of the Reed-Solomon code so as to use a residue or remainder resulting from the division as the error check parity and to assign the error check parity to the last four symbols in the 104-th column. This type of error detection method is known as the cyclic redundancy check code (CRC), and it is described in detail, for example, in Elwyn R. Berkelamp: "ALGEBRAIC CODING THEORY", Chapter 5, pages 119-145, McGraw-Hill Book Company and in W. Wesley Peterson and E. J. Weldon, Jr.: "ERROR-CORRECTING CODES", Second Edition, Chapter 8, pages 206-268.

In the prior art example, in a reproducing operation, the data are arranged, like in the case of the recording operation, in the form having 10 vertical symbols × 104 horizontal symbols. In the respective data symbols in byte unit arranged in the first column through the 103rd column, an addition of respective exclusive OR results of data of ten symbols in each column is performed. In the 104-th column, an addition of respective exclusive OR results of data of six symbols excepting the symbols for the error check parity is performed. Thus, an error check information polynomial for the total 104 data symbols in byte unit is obtained. The information polynomial is divided by the generator polynomial used in the recording operation so as to obtain a residue or remainder. The remainder is then compared with the error detection parity of the 104-th column added in the recording operation and corrected in the reproducing operation, thereby detecting the presence or absence of the error. In this method, for the generation of the information polynomial, an addition of exclusive OR results of data of ten or six symbols in each column is performed. Consequently, there arises a disadvantage that even when a plurality of errors occur in the respective columns, there may possibly be obtained a result identical to the result computed when there does not exist any error. For example, even when two data items having the same bit constitution are included in a column and the same error occurs on bits located at the same positions of the respective data items, it is natural that the same result of the addition of the exclusive OR results of ten symbols is attained for this column in this case and in a case where there does not exist any error in the data item. However, in the error correction method of the data file utilizing the otpical disk of this kind, there are provided error correction codes other than those adopted in the error detection method described above so as to correct an error of each data in advance, thereby greatly minimizing the chance of the operation in which the error described above is not appropriately detected. In the method of the prior art example, with respect to the error correction and the CRC error detection code, the generator polynomial differs, however, the Reed-Solomon code in byte unit of the same primitive polynomial is used, and hence various error detection methods can be considered by combining the error correction code with the CRC error detection code. In the proposal to ANSI X3B11 already described, however, the error detection method has not been presented. In general, the error detection is accomplished in the prior art example as follows. Namely, as described above, in the reproducing operation, firstly, the reproduced data and the error correction parity are arranged in the form having ten vertical symbols × 120 horizontal symbols like in the recording operation, by using 16 parity data items additionally disposed in advance for the error correction of the data associated with 104 user data symbols in a horizontal row, a maximum of eight errors are corrected for each row, and, for each data in byte unit in a range from the first column to the 103rd column, an addition of exclusive OR results of ten symbols in each column is effected and an addition is achieved on exclusive OR results of six-symbol data of the 104-th column excepting the error detection parity so as to obtain an error check information polynomial for the total 104 data symbols in byte unit. The information polynomial is divided by the same generator polynomial used in the recording operation so as to compare the residue with the error correction parity in the 104-th column. If the residue is equal to the parity, it is judged that there does not exist any error. Otherwise, the existence of an error is determined. As the error detection method, there has been adopted a method in which all data items are written in the memory during the reproducing operation as shown in FIG. 1 and thereafter an error correction processing is performed on the data such that the same error detection processing is effected when the data thus corrected are transferred to the user side, for example, a host computer.

In this method, however, a result of the error detection is attained after all data items corrected are entirely transferred to the host computer, which causes a disadvantage in some cases.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an error detection method of detecting a code error in a data file employing an optical disk in which, during a reproducing operation, an error location and an error pattern obtained in an error correction processing are used to correct the data constituting an information polynomial or a reception polynomial, thereby completing the error detection before the data are transferred to the user (host computer).

In order to achieve the above object, there is provided a method according to the present invention in which, in a recording operation, data including user data and control data representing addresses of an optical disk where the data are to be written is arranged in a form with n vertical symbols × m horizontal symbols, an addition is effected on exclusive OR results of n symbols in each vertical column ranging from the first column to the (m - 1)-th column, and an addition is achieved on exclusive OR results of (n - t) symbols of the m-th column excepting t symbols including the last symbols, thereby establishing an information polynomial of data including the m symbols thus obtained. The information polynomial is then divided by a generator polynomial beforehand prepared for an error detection and a residue obtained as a result of the division is arranged as an error detection parity in the t-byte location. In a reproducing operation, if a code error is found in the data of the m symbols of a horizontal row selected from the data constituted with n vertical symbols × m horizontal symbols or in data of (m - 1) symbols excepting the control data, an error correction is accomplished by using an error correction code separately determined and a correction is carried out on the error detecting information polynomial for the data subjected to the error correction based on a location and a pattern associated with the error data obtained in the error correction, thereby detecting an error according to the result of the correction.

In the above configuration, when the error correction is completed on the data in a sector, a code error detection on the corrected data is also completed almost at the same time, and hence the code error detection can be carried out before the data are transferred to the user (host computer) and all processing can be completely effected within a period of time associated with the sector.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram showing a conventional system which performs code error detection on a data file using an optical disk;

FIG. 2 is a block diagram showing a system of an embodiment of the present invention which performs code error detection on a data file using an optical disk; and

FIG. 3 is an explanatory diagram showing a data arrangement for performing code error detection in an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The illustration of FIG. 2 includes a host computer 1, an interface 2, a digital modulation circuit 3, a digital demodulation circuit 4, a sector buffer memory 5, an adder 6 for performing an addition of exclusive OR results of ten symbol data or 6 symbol data used in making code error check, a code error detection code (CRC) generator/checker 7, an error correction circuit 8, an encode/decode change-over switch 9, a data bus 10, an optical disk 11, and a temporary memory 12.

Furthermore, in the data arrangement of FIG. 3, $D_{i,j}$ ($0 \leq i \leq 9$, $0 \leq j \leq 103$) designates user data and control data, $E_{i,k}$ ($0 \leq k \leq 15$) denotes the error correction parity, Cu ($0 \leq u \leq 3$) indicates the error check parity, Pv ($0 \leq v \leq 103$) stands for data constituting an error check information polynomial, and $R_{i,s}$ ($0 \leq s \leq 3$) designates data constituting the residue polynomial of each row.

First, in a recording operation, from the host computer 1, the user data and control data $D_{i,j}$ are supplied as symbols in byte unit via the interface 2 and the data bus 10 to the sector buffer memory 5 in the order of $D_{0,103}$, $D_{1,103}$, $D_{2,103}$, ... , $D_{9,103}$, $D_{0,102}$, ... $D_{9,102}$, ... , $D_{0,1}$, $D_{1,1}$, $D_{2,1}$, ..., $D_{9,1}$, $D_{0,0}$, $D_{1,0}$, $D_{2,0}$, $D_{3,0}$, $D_{4,0}$, and $D_{5,0}$ so as to be stored in the form with ten vertical symbols × 104 horizontal symbols as shown in FIG. 3. At the same time, the data items are supplied to the adder circuit 6, which in turn effects an addition of exclusive OR results as follows.

$$P_{103} = \sum_{i=0}^{9} D_{i,103}$$

$$P_{102} = \sum_{i=0}^{9} D_{i,102}$$

$$\vdots$$

$$P_{1} = \sum_{i=0}^{9} D_{i,1}$$

$$P_{0} = \sum_{i=0}^{5} D_{i,0}$$

These data items represented by Pv ($0 \leq v \leq 103$) are inputted to the CRC generator/checker 7 in the order of P_{103}, P_{102}, ... , P_0 so as to be divided by a predetermined four-symbol generator polynomial G(x). A residue R(x) resulting from the division is produced as error check parity data symbols C_3 to C_0, which are then written in the sector buffer memory 5. Subsequently, data items of a horizontal row including $D_{0,j}$, $D_{1,j}$, ... , $D_{5,j}$ ($0 \leq j \leq 103$); $D_{6,j}$ and C_3,$D_{7,j}$ and C_2, $D_{8,j}$ and C_1, $D_{9,j}$ and C_0 ($1 \leq j \leq 103$) are read out from the sector buffer so as to compute the error correction parity Ei,k in the error correction circuit 8 and the parity Ei,k is then written in the sector buffer memory 5. Finally, the data items of the sector buffer memory 5 are read out in the order of $D_{0,103}$, $D_{1,103}$, $D_{2,103}$, ... , $D_{9,103}$, $D_{0,102}$, $D_{1,102}$, $D_{2,102}$, ... , $D_{9,102}$, ... , $D_{0,1}$, $D_{1,1}$, $D_{2,1}$, ... , $D_{9,1}$, $D_{0,0}$, $D_{1,0}$, $D_{2,0}$, ... , $D_{5,0}$, C_3, C_2, C_1, C_0, $E_{0,15}$, $E_{1,12}$, $E_{2,15}$, ... , $E_{9,15}$, $E_{0,14}$, $E_{1,14}$, $E_{2,14}$, ... , $E_{9,14}$, ... , $E_{0,0}$, $E_{1,0}$, $E_{2,0}$, ... , $E_{9,0}$ so as to be supplied via the encode/decode switch 9 to the digital modulation circuit 3, which in turn adds signals such as a synchronization signal and records the resultant data items on the optical disk 11.

On the other hand, in a reproducing operation, data items read from the optical disk 11 are demodulated by the digital demodulation circuit 4 and are supplied via the encode/decode switch 9 to the sector buffer memory 5. The data items are written therein in the form with ten vertical symbols × 120 horizontal symbols, like in the recording operation, as shown in FIG. 3. At the same time, the data items are inputted to the adder 6, which then performs an addition of exclusive OR results as follows.

$$\hat{P}_{103} = \sum_{i=0}^{9} \hat{D}_{i,103}$$

$$\hat{P}_{102} = \sum_{i=0}^{9} \hat{D}_{i,102}$$

$$\vdots$$

$$\hat{P}_{0} = \sum_{i=0}^{5} \hat{D}_{i,0}$$

Where, $\hat{}$ indicates that the data bearing this mark appear in a reproducing operation. These data $\hat{P}v$ (0

≤ v ≤ 103) are written in a temporary memory 12. Next, the data $D_{0,j}$ (0 ≤ j ≤ 103) and $E_{0,k}$ (0 ≤ k ≤ 15) are sequentially read out in the direction from the left side to the right side in FIG. 3 and are supplied to the error correction circuit 8. In the error correction circuit 8, a location and a pattern of the error are computted. Then, data corresponding to the error location are read from the sector buffer memory 5 and are inputted to the error correction circuit 8. Thereafter, an addition of exclusive OR results is effected for the error pattern and the above data, and the resultant data are written again in the sector buffer memory 5 at the original address, thereby effecting the error correction. Subsequently, $\hat{P}v$ corresponding to the error location is read from the temporary memory 12 and is then supplied to the error correction circuit 8. An addition of exclusive OR results is effected for the error pattern and the above data, and the resultant data are written again in the temporary memory 12 at the original address. Then, the above operation is repeated for i (1 ≤ i ≤ 9) and thus it is repeated ten times in total. Finally, the data are read from the temporary memory 12 in the order of $\hat{\hat{P}}_{103}$, $\hat{\hat{P}}_{102}$, ... , $\hat{\hat{P}}_{1}$, and $\hat{\hat{P}}_{0}$ and are inputted to the CRC generator/checker 7, which conducts a division thereof by a predetermined generator polynomial G(x) that has also been used in the recording operation. An explanation of the mark $\hat{\ }$ soon follows. As a result, the residue $\mathring{R}(x)$ is attained as $\mathring{C}_3$ to $\mathring{C}_0$, which are compared with the error correction parity $\hat{\hat{R}}$ (x) subjected to the error correction, namely, $\hat{\hat{C}}_3$ to $\hat{\hat{C}}_0$ read from the sector buffer memory 5 and supplied to the CRC generator/checker 7. If a matching condition results, the system determines that there does not exist any error. Otherwise, the existence of an error is assumed. When the error is not found in this judgement, from the sector buffer memory 5, the user data Di,j are transferred via the data bus 10 and the interface 2 to the host computer 1. When the error is assumed, an error message is transmitted to the host computer 1. In the above description, the mark $\hat{\ }$ designates data that have been subjected to error correction in the reproducing operation, and the mark * indicates data obtained through a computation after the error correction. In this case, as the generator polynomial G(x) of the error check parity, the following is used when the primitive element of the finite field or Galois field obtained through a primitive polynomial $m(x) = x^8 + x^4 + x^3 + x^2 + 1$ is assumed to be α.

$$G(x) = \prod_{i=0}^{3} (x + \alpha^i)$$

Alternatively, as the generator polynomial G(x) of the error check parity, the following is used when the primitive element of the finite field or Galois field obtained through a primitive polynomial $m(x) = x^8 + x^5 + x^3 + x^2 + 1$ is assumed to be α.

$$G(x) = \prod_{i=136}^{139} (x + \alpha^{88i})$$

Here, the generator polynomial G(x) is in byte unit. However, the generator polynomial G(x) need not be necessarily associated with the byte unit, for example, there may also be employed $G(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$ associated with the binary unit. In a case where the byte-unit generator polynomial is used, the error check parity Cu is here computed so as to satisfy the following expression.

$$R(x) = C_0, C_1, C_2, C_3$$

$$= \left[\{ (\sum_{i=0}^{9} D_{i,103}) \cdot x^{103} + (\sum_{i=0}^{9} D_{i,102}) \cdot x^{102} \ \ldots \right.$$

$$\left. \ldots + (\sum_{i=0}^{9} D_{i,1}) \cdot x + (\sum_{i=0}^{5} D_{i,0}) \} \cdot x^4 \right] \bmod \prod_{i=0}^{3} (x+\alpha^i)$$

or

$$R(x) = C_0, C_1, C_2, C_3$$

$$= \left[\{ (\sum_{i=0}^{9} D_{i,103}) \cdot x^{103} + (\sum_{i=0}^{9} D_{i,102}) \cdot x^{102} \ \ldots \right.$$

$$\left. \ldots + (\sum_{i=0}^{9} D_{i,1}) \cdot x + (\sum_{i=0}^{5} D_{i,0}) \} \cdot x^4 \right] \bmod \prod_{i=136}^{139} (x+\alpha^{88i})$$

When using a binary-unit generator polynomical, the residue is obtained in the same way as the conventional method on assumption that the 8 bit data including

$$(\sum_{i=0}^{9} D_{i,103}), (\sum_{i=0}^{9} D_{i,102}), \ldots . , \text{and}$$

$$(\sum_{i=0}^{5} D_{i,0})$$

are continuous bit streams, respectively, and then the result need only be divided into 8 bit units.

In addition, in place of the operation as described above in which the error check parity $\hat{\hat{R}}(x)$, namely, $\hat{\hat{C}}_3$ to $\hat{\hat{C}}_0$ that are computed and are added in the recording operation and that are subjected to the error correction processing are compared with $\hat{R}(X)$, namely, $\hat{C}_3$ to $\hat{C}_0$ attained through a computation in the reproducing operation so as to judge the presence or absence of the error, it is possible to supply the CRC generator/checker 7 with $\hat{P}u$ from the temporary memory 12 and R(x) from the sector buffer memory 5 in the sequence of $\hat{\hat{P}}_{103}$, $\hat{\hat{P}}_{102}$, ... , $\hat{\hat{P}}_0$, $\hat{\hat{C}}_3$, $\hat{\hat{C}}_2$, $\hat{\hat{C}}_1$, and $\hat{\hat{C}}_0$ so as to be divided by the generator polynomial G(x), thereby determining the presence or absence of an error from the fact that the residue is not 0 or 0, respectively.

Next, a second embodiment of this invention will be explained.

In the first embodiment, the data items constituting the error check information polynomial are beforehand generated through an addition of exclusive OR results of the ten byte or 6 byte reproduction data in the column direction of FIG. 3 and thereafter by using the error location and the error pattern obtained during the error correction associated with each row, a correction is also effected on the data items constituting the information polynomical so as to accomplish the error detection. In contrast with the first embodiment, according to the second embodiment, an error correction is first performed on data in an N-th row of FIG. 3, and an addition of exclusive OR results of the data of the N-th row thus corrected and the data of the (N + 1)-th row not corrected is conducted for each symbol located in the same column so as to generate data items constituting a provisional information polynomial. Subsequently, error corrections are repeatedly performed on the data of the (N + 1)-th row and the data items associated with the

provisional information polynomial so as to effect a correction of the information polynomial, thereby carrying out the error detection. In this situation, the operation to record the data is the same as that of the first embodiment. In the recording operation, data read from the optical disk 11 are demodulated by the digital demodulation circuit 4 and are then written via the encode/decode change-over switch 9 in the sector buffer memory 5 in the data arrangement, like in the recording operation, constituted by ten vertical symbols × 120 horizontal symbols as shown in FIG. 3. Next, the data and the error correction parity including $\hat{D}_{0,103}$, $\hat{D}_{0,102}$, ... , $\hat{D}_{0,0}$, $\hat{E}_{0,15}$, ... , and $\hat{E}_{0,0}$ of the upper-most row of FIG. 3 are read from the sector buffer memory 5 and are then supplied to the error correction circuit 8. At the same time, data items $\hat{D}_{0,103}$, $\hat{D}_{0,102}$, ... , and $\hat{D}_{0,0}$ are written in the temporary memory 12. In the error correction circuit 8, the location and the pattern of the error are computed for the error correction. Thereafter, the error data corresponding to the error location are read from the temporary memory 12 and are delivered to the error correction circuit 8, which then effects an addition of exclusive OR results of the error pattern and the data thus read out, thereby performing the error correction. The resultant data are written again in the temporary memory 12 at the original address. In this operation, in the error correction circuit 8, the data $\hat{D}_{0,103}$ is inputted to an input terminal of a syndrome generator and to an input terminal of an exclusive OR circuit. At the same time, the corrected data $\hat{\hat{D}}_{0,103}$ is read from the temporary memory 12 and is supplied to the other input terminal of the exclusive OR circuit of the error correction circuit 8, and then a computation of $\hat{P}_{103} = \hat{D}_{0,102} \oplus \hat{\hat{D}}_{0,103}$ is accomplished, and the obtained data are written again in the temporary memory 12 at the original address. Subsequently, in a similar way, while $\hat{D}_{0,102}$, $\hat{D}_{0,101}$, ... , and $\hat{D}_{0,0}$ are sequentially supplied to the syndrome generator and the exclusive OR circuit, computations of $\hat{P}_{102} = \hat{D}_{0,102} \oplus \hat{\hat{D}}_{0,102}$, $\hat{P}_{101} = \hat{D}_{0,10,} \oplus \hat{\hat{D}}_{0,101}$, ... , and $\hat{P}_0 = \hat{D}_{0,0} + \hat{\hat{D}}_{0,0}$ are effected and the resultant data items are written again in the temporary memory 12 at the respective original addresses. After these operations are completed, the error location and the error pattern are computed for the data and the error check parity in the second row of FIG. 3. Data corresponding to the error location are read from the sector buffer memory 5 and are then delivered to the error correction circuit 8, which in turn effects an addition of exclusive OR results of the error pattern and the data thus read out, thereby achieving the error correction. The resultant data are written again in the sector buffer memory 5 at the original address. Subsequently, $\hat{P}u$ corresponding to the error location are read from the temporary memory 12 and are fed to the error correction circuit 8, which in turn effects an addition of exclusive OR results of the error pattern and the data of $\hat{P}u$ thus read out, thereby performing the error correction. The resultant data are written again in the temporary memory 12 at the original address. Following this operation, for the data from the third row to the tenth row, the similar processing is repetitiously carried out. When the error correction and the correction of data items constituting the information polynomial for the CRC computation are completed for the data of tenth row, there are obtained in the temporary memory 12 the data items constituting the information polynomial for the CRC computation which data items are identical to those of the first embodiment.

Next, a third embodiment of the present invention will be explained.

In the third embodiment different from the first and second embodiments, in a reproducing operation, the data read from the optical disk 11 are written in the sector buffer memory 5, like in the recording operation, to form a shape constituted by ten vertical symbols × 120 horizontal symbols. Next, the data and the error correction parity of the first horizontal row of the upper-most line of FIG. 3 including $\hat{D}_{0,103}$, $\hat{D}_{0,102}$, ... , $\hat{D}_{0,0}$, $\hat{E}_{0,15}$, ... , and $\hat{E}_{0,0}$ are read from the sector buffer memory 5 and are then inputted to the error correction circuit 8, which in turn effects an error correction for the received data and parity. The corrected data are thereafter written again in the sector buffer memory 5 at the original address. Subsequently, the corrected data $\hat{\hat{D}}_{0,103}$, $\hat{\hat{D}}_{0,102}$, ... , and $\hat{\hat{D}}_{0,0}$ are read from the sector buffer memory 5 so as to be supplied to the CRC generator/checker 7, which divides the data by a predetermined generator polynomial G(x) to obtain a residue $\hat{R}_0(x)$, namely, $\hat{C}_{0,3}$, $\hat{C}_{0,2}$, $\hat{C}_{0,1}$, and $\hat{C}_{0,0}$ to be stored in the temporary memory 12. Similarly, for the rows ranging from the second row to the sixth row, there is obtained a residue for each column, namely, $\hat{R}_1(x)$ to $\hat{R}_5(x)$ including $\hat{C}_{1,3}$, $\hat{C}_{1,2}$, $\hat{C}_{1,1}$, $\hat{C}_{1,0}$, ... , $\hat{C}_{5,3}$, $\hat{C}_{5,2}$, $\hat{C}_{5,1}$, $\hat{C}_{5,0}$, which are then written in the temporary memory 12.

In the almost similar fashion, the residue is obtained for each of the rows ranging from the seventh row to the tenth row, which is different from that of each of the rows ranging from the first row to the sixth row. Namely, as can be seen from FIG. 3, the number of data items of each row is smaller than that of each row associated with the rows ranging from the first row to the sixth row by one symbol and hence the computation is carried out on assumption that ø data exists in that location. In this fashion, there are obtained the residues $\hat{R}_6(x)$ - $\hat{R}_9(x)$, namely, $\hat{C}_{6,3}$, $\hat{C}_{6,2}$, $\hat{C}_{6,1}$, $\hat{C}_{6,0}$ to $\hat{C}_{9,3}$, $\hat{C}_{9,2}$, $\hat{C}_{9,1}$, $\hat{C}_{9,0}$. Finally, an addition of the exclusive OR results is effected on $\hat{R}_0(x)$ to $\hat{R}_9(x)$ as follows.

$$\dot{R}(x) = \dot{R}_1(x) \oplus \dot{R}_2(x) \oplus .... \oplus \dot{R}_9(x) = \sum_{i=0}^{9} \dot{R}_i(x)$$

$$\dot{C}_3 = \dot{C}_{0,3} \oplus \dot{C}_{1,3} \oplus ... \oplus \dot{C}_{9,3}$$

$$\dot{C}_2 = \dot{C}_{0,2} \oplus \dot{C}_{1,2} \oplus ... \oplus \dot{C}_{9,2}$$

$$\dot{C}_1 = \dot{C}_{0,1} \oplus \dot{C}_{1,1} \oplus ... \oplus \dot{C}_{9,1}$$

$$\dot{C}_0 = \dot{C}_{0,0} \oplus \dot{C}_{1,0} \oplus ... \oplus \dot{C}_{9,0}$$

The error detection after this point is identical to that described in conjunction with the second embodiment.

It is necessary here to prove that the residues of the first and embodiment are equal to those of the third embodiment. For simplification of the description, it is assumed that there does not exist any error in a reproducing operation. Naturally, the essential properties are not lost by the above assumption.

In the embodiment of FIG. 3, the following expressions are obtained by assuming that the information polynomial and the generator polynomial of the first row of FIG. 3 are Mi(x) and G(x), respectively, and that the quotient polynomial and the residue polynomial obtained by dividing the information polynomial Mi(x) by the generator polynomial G(x) are Qi(x) and Ri(x), respectively.

$$R_0(x) = x^4 \cdot M_0(x) + Q_0(x)\ G(x)$$

$$R_1(x) = x^4 \cdot M_1(x) + Q_1(x)\ G(x)$$

$$\vdots$$

$$R_9(x) = x^4 \cdot M_9(x) + Q_9(x)\ G(x)$$

Assume here that an addition of the data $R_0(x)$ to $R_9(x)$ is represented by $Rc(x)$, namely,

$$R_c(x) = \sum_{i=0}^{9} R_i(x) = x^4 \cdot \sum_{i=0}^{9} M_i(x) + G(x) \cdot \sum_{i=0}^{9} Q_i(x)$$

where,

$$M_0(x) = D_{0,103} \cdot x^{103} + D_{0,102} \cdot x^{102} + ... + D_{0,1} \cdot x + D_{0,0}$$

$$M_1(x) = D_{1,103} \cdot x^{103} + D_{0,102} \cdot x^{102} + ... + D_{1,1} \cdot x + D_{1,0}$$

$$\vdots$$

$$M_5(x) = D_{5,103} \cdot x^{103} + D_{5,102} \cdot x^{102} + ... + D_{5,1} \cdot x + D_{5,0}$$

$$M_0(x) = D_{6,103} \cdot x^{103} + D_{6,102} \cdot x^{102} + ... + D_{6,1} \cdot x$$

$$\vdots$$

$$M_9(x) = D_{9,103} \cdot x^{103} + D_{9,102} \cdot x^{102} + ... + D_{9,1} \cdot x$$

Here, the following relationship is satisfied in the first embodiment.

$$M(x) = (D_{0,103} \oplus D_{1,103} \oplus \cdots \oplus D_{9,103}) \cdot x^{103} + (D_{0,102} \oplus D_{1,102} \oplus \cdots \oplus D_{9,102}) \cdot x^{102} + - - - - - - - - - - - - - - - - + (D_{0,1} \oplus D_{1,1} \oplus \cdots \oplus D_{9,1}) \cdot x + (D_{0,0} \oplus D_{1,0} \oplus \cdots \oplus D_{5,0}) = \sum_{i=0}^{9} Mi(x)$$

Consequently, the error check parity, namely, the residue polynomial of the first embodiment is expressed as follows.

$R_D(x) = x^4 \cdot M(x) + Q_D(x)\, G(x)$

Let us check whether or not $Rc(x) = R_D(x)$ is satisfied.

$$R_C(x) - R_D(x) = x^4 \cdot \sum_{i=0}^{9} Mi(x) + G(x) \cdot \sum_{i=0}^{9} Qi(x) - x^4 \cdot M(x) - Q_D(x)\, G(x) = \left(\sum_{i=0}^{9} Qi(x) - Q_D(x) \right) G(x)$$

Assuming here that G(x) is a polynomial of t degree, the expression on the left side is a polynomial of t-1 degree at most. On the other hand, if

$$\left(\sum_{i=0}^{9} Q_i(x) - Q_D(x) \right) \neq 0,$$

the expression on the right side becomes a polynomial of degree t or more, which is inconsistent with the t-1 degree on the left side. Consequently,

$$\left(\sum_{i=0}^{9} Q_i(x) - Q_D(x) \right) = 0$$

must be satisfied. As a result, $Rc(x) = R_D(x)$ is attained. That is, the error check parity of the first embodiment is identical to that of the third embodiment.

According to the third embodiment, after the error correction is performed on the data of each horizontal row of FIG. 3 so as to obtain the error check parity of each horizontal row, an addition of

exclusive OR results is effected for the error check parity obtained for each horizontal row so that the result of the addition is compared with the error check parity obtained in the recording operation, thereby detecting the presence or absence of the error. Consequently, a relatively long period of time is required to accomplish the computation. Next, an embodiment for improving the above operation will be described.

In this embodiment, the data of a horizontal row of FIG. 3 are transferred from the sector buffer memory 5 to the error correction circuit 8, and then after the error correction is completed, the corrected data are written again in the sector buffer memory 5 at the original address. Subsequently, the data of the second row are transferred from the sector buffer memory 5 to the error correction circuit 8, and then after the error correction is completed, the corrected data are written again in the sector buffer memory 5 at the original address. According to the error correction procedure in this embodiment, a syndrome is computed by using the data first transferred from the sector buffer memory 5. Next, based on the syndrome thus obtained, the error location polynomial and error evaluator polynomial are computed so as to obtain the error location and the error pattern therefrom. Error data corresponding to the error location are read from the sector buffer memory 5 and then an addition of exclusive OR results is effected between the error data and the error pattern so as to perform the error correction, thereby writing again the corrected data in the sector buffer memory 5 at the original address. In this operation, the sector buffer memory 5 is accessed only when the data of a horizontal row are transferred to the error correction circuit 8 to obtain the syndrome, when the error data are read out, and when the corrected data are rewritten. Namely, since the sector buffer memory 5 is not accessed when the error correction circuit 8 is computing the error location and the error pattern, this period of time is allocated to an operation to read from the sector buffer memory 5 the corrected data of the first row of FIG. 3 including $\hat{\hat{D}}_{0,103}$, $\hat{\hat{D}}_{0,102}$, ... , and $\hat{\hat{D}}_{0,0}$, which are then inputted to the CRC generator/checker 7. In the CRC generator/checker 7, the data items are subdivided by the generator polynomial G(x) and the residue $\hat{R}_0(x)$ is obtained as $\hat{C}_{0,3}$, $\hat{C}_{0,2}$, $\hat{C}_{0,1}$, and $\hat{C}_{0,0}$ so as to be written in the temporary memory 12. In the similar fashion, the error correction up to the tenth row is effected and $\hat{C}_{1,3}$, $\hat{C}_{1,2}$, $\hat{C}_{1,1}$, $\hat{C}_{1,0}$, ... , $\hat{C}_{8,3}$, $\hat{C}_{8,2}$, $\hat{C}_{8,1}$ and $\hat{C}_{8,0}$ as the residues $\hat{R}_1(x)$ to $\hat{R}_8(x)$ up to the ninth row are obtained, and they are written in the temporary memory 12.

Finally, the corrected data items $\hat{\hat{D}}_{9,103}$, $\hat{\hat{D}}_{9,102}$, ... , $\hat{\hat{D}}_{9,0}$ of the tenth row are read from the sector buffer memory 5 so as to be supplied to the CRC generator/checker 7. In the CRC generator/checker 7, the residue $\hat{R}_9(x)$ is obtained as $\hat{C}_{9,3}$, $\hat{C}_{9,2}$, $\hat{C}_{9,1}$, and $\hat{C}_{9,0}$. Next, the residues $\hat{R}_0(x)$ to $\hat{R}_9(x)$ are read from the temporary memory and are then inputted to the error correction circuit 8, which performs an addition of exclusive OR results of the residues $\hat{R}_0(x)$ to $\hat{R}_9(x)$ to thereby obtain the final error check parity data $\hat{C}_3$, $\hat{C}_2$, $\hat{C}_1$, and $\hat{C}_0$. These error check parity data are compared with the error check parity data $\hat{\hat{C}}_3$, $\hat{\hat{C}}_2$, $\hat{\hat{C}}_1$, and $\hat{\hat{C}}_0$ which have been added to the 104-th column shown in Fig. 3 in the recording operation and for which error correction has been effected in the reproducing operation, thereby accomplishing the error detection. In an error correction code system, like that discussed in the present invention, which deals with an error correction code whose minimum inter-code distance is as great as 17, the processing to compute the error location and the error pattern requires relatively a long period of time. That is, the period of time associated with the processing above is sufficient for the system to read the data of a horizontal row from the sector buffer memory 5 and to transfer the data to the CRC generator/checker 7 so as to effect the processing. Furthermore, this method is of course applicable to the error check parity generation in the recording operation, if it is assumed that any error does not exist exactly in the reproducing operation.

Now, as already described with respect to the prior art example, in the method of producing an information polynomial by performing an addition of exclusive OR results of ten vertical symbols in each column among the data arranged in the form having ten vertical symbols and 104 horizontal symbols, if an even number of errors should occur at the same bit positions of the data having the same bit structure in a column, an addition of exclusive OR results of the ten vertical symbols in the column becomes completely identical to that obtained when there exists no error. Similarly, in an error detection method in which error correction is performed for each horizontal row so as to obtain an information polynomial by using data resulting therefrom, the information polynomial thus obtained is then divided by a generator polynomial to obtain a residue polynomial for each row, and finally the residue polynomials for respective rows are added together to effect error detection, for example, if all data in two rows are identical with each other and identical errors should occur at the same positions thereof, the two resultant residue polynomials become completely identical with each other, namely, an addition of exclusive OR results therefrom becomes identical to that obtained when there does not exist any error. In these cases, it results that the existence of such errors is overlooked. Although it is considered that such cases stand generally with low probability, if two separate code error detection methods are used in parallel to decide the existence of an error and if the existence of an error is detected by any one of the two methods, it is possible to assure high reliability.

While the present invention has been described with reference to the particular embodiments, it is not

restricted by those embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change and modify the embodiments without departing from the scope and spirit of the present invention.

Claims

1. A code error detecting method, wherein

an information polynomial of the i-th code word of n sets of Reed-Solomon codes constituted by m data symbols ($D_{i,j}$) each constituted by h binary bits and (g - m) error correction parity symbols ($E_{i,k}$) is denoted by Mi(x),

a generator polynomial of t degree for t error check parity symbols constituted by h binary bits is denoted by G(x),

a quotient polynomial and a residue polynomial obtained by dividing the information polynomial Mi(x) by the generator polynomial G(x) are denoted by Qi(x) and Ri(x), respectively,

an addition of exclusive OR results of the information polynomial is represented by

$$M(x) = \sum_{i=0}^{n-1} Mi(x),$$

an addition of exclusive OR results of the residue polynomial is represented by

$$R(x) = \sum_{i=0}^{n-1} Ri(x),$$

and

respective degree terms (C_3, C_2, C_1, C_0) of the residue polynomial $R_i(x)$ obtained by $x^t \cdot M_i(x)/G(x)$ are inserted in the ø degree position of the information polynomial Mi(x) of the code words of the n sets of Reed-Solomon codes, in the order of i = n-1, i = n-2, and so forth sequentially from ø degree term;

then, in a reproducing operation, the i-th information polynomial obtained in the reproducing operation is denoted by $\hat{M}_i(x)$,

An information polynomial obtained by correcting $\hat{M}_i(x)$ by error correction parity simbols ($E_{i,k}$) constituted by (g - m) Reed-Solomon codes is denoted by $\hat{\hat{M}}_i(x)$,

a quotient polynomial and a residue polynomial obtained by dividing $\hat{\hat{M}}_i(x)$ by the generator polynomial G(x) are denoted by $\hat{Q}_i(x)$ and $\hat{R}_i(x)$, respectively,

an addition of exclusive OR results of the information polynomials $\hat{M}_i(x)$ is represented by $\hat{M}(x) =$

$$\sum_{i=0}^{n-1} \hat{M}i(x),$$

and

an addition of exclusive OR results of the residue polynomials $R_i(x)$ is represented by $\hat{R}(x) =$

$$\sum_{i=0}^{n-1} Ri(x);$$

whereby, when a residue polynomial obtained by correcting coefficients ($\hat{C}_3$, $\hat{C}_2$, $\hat{C}_1$, $\hat{C}_0$) of the respective degrees of a residue polynomial R(x) resulting from the reproduction of the residue polynomial R(x), by using error correction parity symbols ($E_{i,k}$) constituted by (g - m) Reed-Solomon codes, is denoted by $\hat{\hat{R}}(x)$,

a decision is made that there exists no error, if $\hat{R}(x) = \hat{\hat{R}}(x)$ holds, and

a decision is made there exists an error, if $\hat{R}(x) \neq \hat{\hat{R}}(x)$ holds.

2. A code error detecting method according to Claim 1, wherein
a decision is made that there exists no error, if

$$x^t \cdot \hat{\hat{M}}(x) + \hat{\hat{R}}(x) = G(x) \cdot \sum_{i=0}^{n-1} \dot{Q}_i(x) + \dot{R}(x) + \hat{\hat{R}}(x) = 0$$

holds, and
a decision is made that there exists an error, if

$$X^t \cdot \hat{\hat{M}}(x) + \hat{\hat{R}}(x) = G(x) \cdot \sum_{i=0}^{n-1} \dot{Q}_i(x) + \dot{R}(x) + \hat{\hat{R}}(x) \neq 0$$

holds.

3. A code error detecting method, wherein
when symbol data Di,j are arranged in the form including n vertical symbols and m horizontal symbols, an addition of exclusive OR results of n data symbols in each of the columns from the first column to the (m - 1)-th column is performed as represented by

$$\sum_{i=1}^{n-1} \hat{D}i,m-1, \quad \sum_{i=1}^{n-1} \hat{D}i, m-2, \ \ldots\ , \quad \sum_{i=0}^{n-1} \hat{D}i,1,$$

and, in the m-th column, an addition of exclusive OR results of (n - t) symbols excepting t error check parity symbols ($\hat{C}_3$, $\hat{C}_2$, $\hat{C}_1$, $\hat{C}_0$)is performed as represented by

$$\sum_{i=0}^{n-t-1} D_{i,0},$$

thereby producing an information polynomial constituted by m data symbols in total, then, by using an error location and an error pattern obtained through an error correction processing performed per each horizontal row, an addition of exclusive OR results of said error pattern and a data symbol of the information polynomial corresponding to said error location is made so as to effect correction of the information polynomial,
a comparison is made between coefficients [($\dot{C}_3$, $\hat{\hat{C}}_3$), ($\dot{C}_2$, $\hat{\hat{C}}_2$), ($\dot{C}_1$, $\hat{\hat{C}}_1$), ($\dot{C}_0$, $\hat{\hat{C}}_0$)] of respective degrees of a residue polynomial resulting from the devision of the information polynomial thus corrected by a generator polynomial and of a residue polynomial computed in a recording operation and corrected in a reproducing operation,
whereby a decision is made that there exists no error, if coincidence occurs between all paired coefficients, and
a decision is made that there exists an error, if coincidence does not occur in any one of the paired coefficients.

4. A code error detecting method, wherein
in symbol data ($D_{i,j}$) arranged in the form including n vertical symbols and m horizontal symbols, error correction of data in the i-th row is made,
an addition of exclusive OR results is effected between data of the i-th row thus corrected and data of the (i + 1)-th row not yet corrected, both in the same column, so as to produce data constituting a provisional information polynomial, then, by using an error location and an error pattern obtained through error correction of the data of the (i + 1)-th row an addition of exclusive OR results of said error pattern and a data symbol of the provisional information polynomial corresponding to said error location is made so as to effect correction of the information polynomial, and this processing is repeated,
a comparison is made between coefficients [($\dot{C}_3$, $\hat{\hat{C}}_3$), ($\dot{C}_2$, $\hat{\hat{C}}_2$), ($\dot{C}_1$, $\hat{\hat{C}}_1$), ($\dot{C}_0$, $\hat{\hat{C}}_0$)] of respective degrees of a residue polynomial resulting from the division of a finally obtained information polynomial by a

generator polynomial and of a residue polynomial computed in a recording operation and corrected in a reproducing operation,

whereby a decision is made that there exists no error, if coincidence occurs between all paired coefficients, and

a decision is made that there exists an error, if coincidence does not occur in any one of the paired coefficients.

5. A code error correcting method, wherein

error correction is made of the i-th code word in the code words of n sets of Reed-Solomon codes constituted by m data symbols ($D_{i,j}$) and (g - m) error correction parity symbols ($E_{i,k}$),

an information polynomial $\hat{\hat{M}}_{1i}(x)$ constituted by the m data symbols is divided by a generator polynomial G(x) to obtain a residue polynomial $\hat{R}_{1i}(x)$, and this processing is repeated (n - t) times,

an information polynomial $\hat{\hat{M}}_{2i}(x)$ having, as a coefficient of zero degree, (m - 1) data symbols among the m data symbols, excluding a symbol, respectively, from the parity symbols ($\hat{\hat{C}}_3$, $\hat{\hat{C}}_2$, $\hat{\hat{C}}_1$, $\hat{\hat{C}}_0$), which are coefficients of respective degrees of a residue polynomial $\hat{\hat{R}}(x)$ which is an error check parity computed in a recording operation and corrected in a reproducing operation, and symbols constituted by m binary bits "0" is divided by the generator polynomial G(x) to obtain a residue polynomial $\hat{R}_{2i}(x)$, and this processing is repeated t times so as to perform an addition of exclusive OR results of the residue polynomials as represented by

$$R(x) = \sum_{i=0}^{n-t-1} R_{1i}(x) + \sum_{i=n-t}^{n-1} R_{2i}(x),$$

whereby a decision is made that there exists no error, if $\hat{R}(x) = \hat{\hat{R}}(x)$ holds, and

a decision is made that there exists an error, if $\hat{R}(x) = \hat{\hat{R}}(x)$ holds.

6. A code error detecting method according to Claim 5, wherein, while an operational processing of an error location and an error pattern is effected at the time of error correction of the i-th code word, an information polynomial constituted by m corrected data symbols of the (i - 1)-th code word is divided by a generator polynomial so as to obtain a residue polynomial.

7. A code error correcting method which combines the code error detecting method of Claim 3 with the code error detecting method of Claim 5, whereby a decision is made that there exists an error, if the existence of an error is detected by any one of said code error detecting methods.

8. A code error correcting method which combines the code error detecting method of Claim 3 with the code error detecting method of Claim 6, whereby a decision is made that there exists an error, if the existence of an error is detected by any one of said code error detecting methods.

9. A code error correcting method which combines the code error detecting method of Claim 4 with the code error detecting method of Claim 5, whereby a decision is made that there exists an error, if the existence of an error is detected by any one of said code error detecting methods.

10. A code error correcting method which combines the code error detecting method of Claim 4 with the code error detecting method of Claim 6, whereby a decision is made that there exists an error, if the existence of an error is detected by any one of said code error detecting methods.

11. A code error detecting method according to Claim 1, wherein

the generator polynomial (G(x)) of ht degree constituted by binary bits is used, and,

when a residue polynomial is expressed by $C_{ht-1}x^{ht-1} + C_{ht-2}x^{ht-2} + ... + C_1x + C_0$, then ($C_{ht-1}$, C_{ht-2}, ... , C_{ht-8}), ... , (C_{ht-9}, C_{ht-10}, ... , C_{ht-16},) ... , (C_7, C_8, ... C_0) are deemed to be t error check parity symbols which are respectively constituted by h binary bits.

12. A code error detecting method according to any one of Claims 1 to 10, wherein, when a decision is made that there exists an error, an error code (flag) is transferred to a host computer (1) without transferring data thereto.

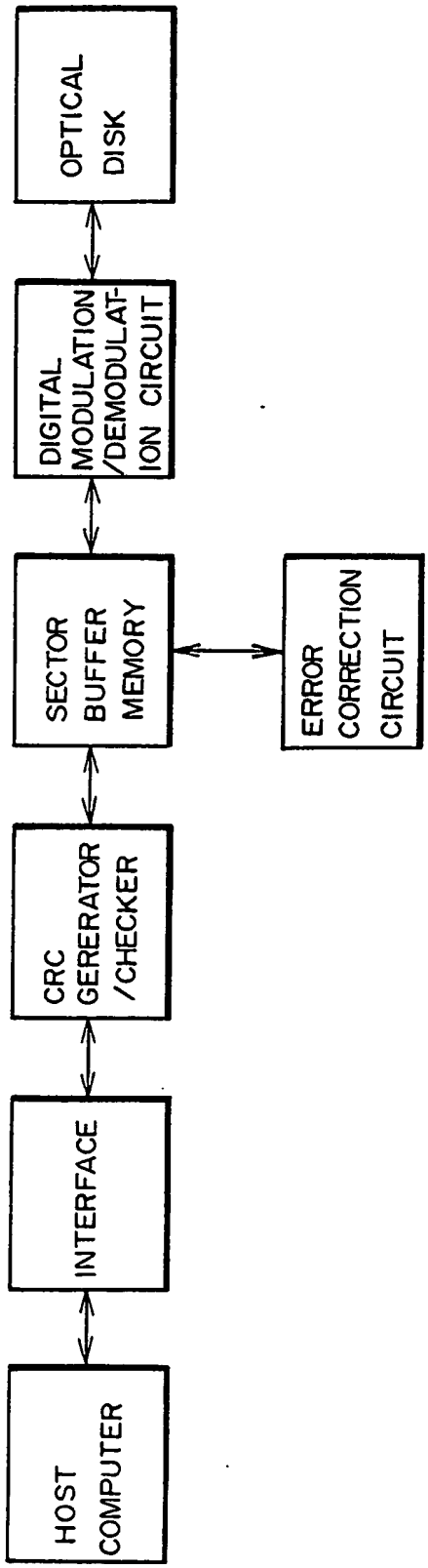


FIG. 1
PRIOR ART

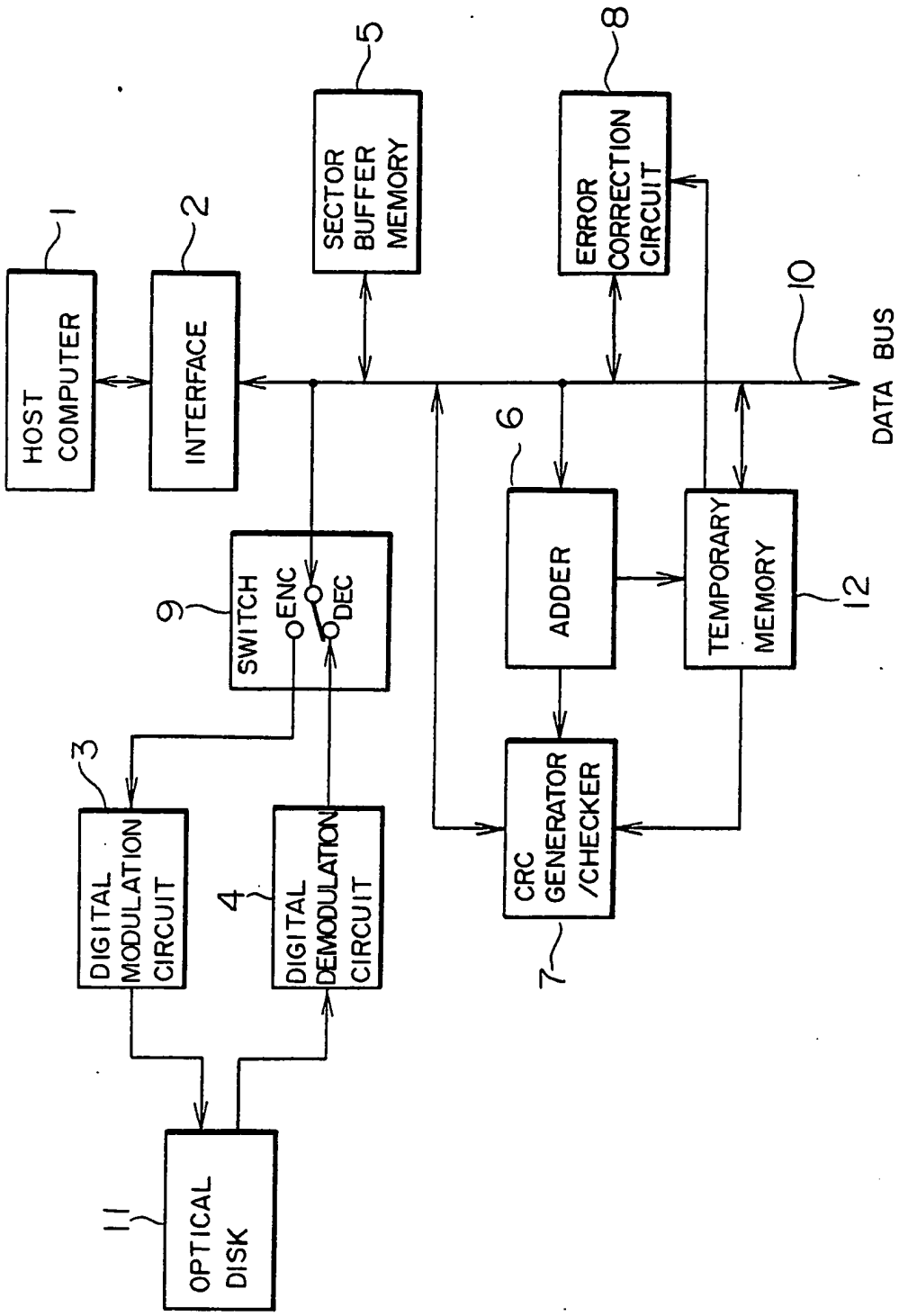
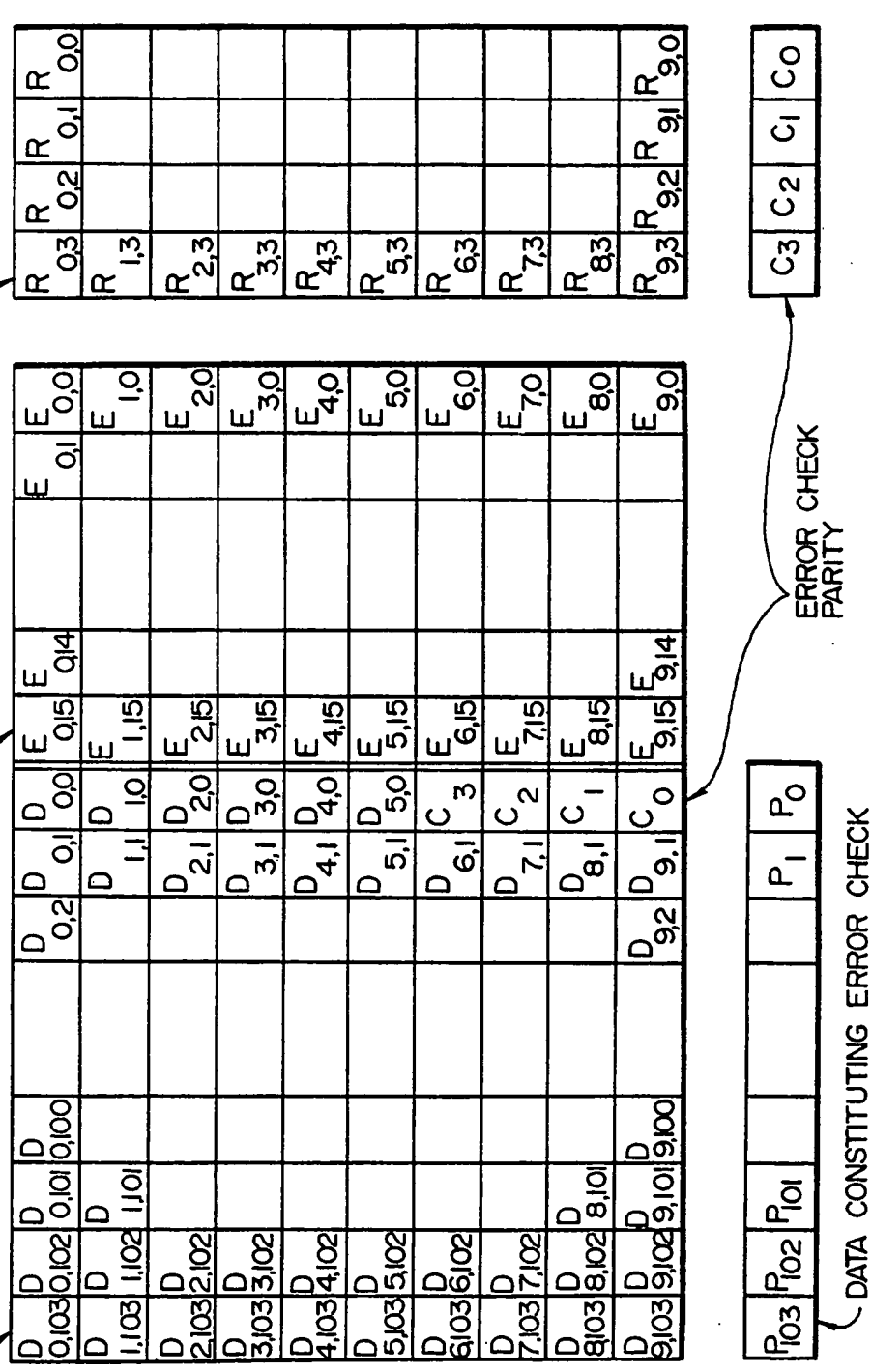

HOST COMPUTER
1
INTERFACE
2
SECTOR BUFFER MEMORY
5
ERROR CORRECTION CIRCUIT
8
10
DATA BUS
6
ADDER
TEMPORARY MEMORY
12
9
SWITCH
ENC
DEC
3
DIGITAL MODULATION CIRCUIT
4
DIGITAL DEMODULATION CIRCUIT
CRC GENERATOR /CHECKER
7
11
OPTICAL DISK

FIG. 2

FIG. 3


USER DATA AND CONTROL DATA
ERROR CORRECTION PARITY
DATA CONSTITUTING REIDUE POLYNOMIAL OF EACH ROW
ERROR CHECK PARITY
DATA CONSTITUTING ERROR CHECK INFORMATION POLYNOMIAL